CLAIMS

What is claimed is:

1. A logic circuit to perform an exclusive or (XOR) logic function without the logic circuit entering an unstable state comprising:

an input circuit to convert a plurality of static input signals to a plurality of complimentary dual-rail domino output signals having one or more valid states; and

an output circuit to perform a plurality of said XOR logic functions on said plurality of complimentary dual-rail domino output signals without the logic circuit entering the unstable state.

2. The logic circuit of claim 1, wherein said output circuit comprises a plurality of XOR logic circuits coupled in parallel to perform said plurality of said XOR logic functions on said plurality of complimentary dual-rail domino output signals.

3. The logic circuit of claim 2, wherein each of said plurality of XOR logic circuits comprises a dual-rail dynamic domino logic circuit having a first pull-down stack and a second pull-down stack coupled in parallel between a ground node and a dynamic node to perform said XOR logic function.

4. The logic circuit of claim 2, further comprising a logic circuit that performs a logical 'NAND' function on a plurality of outputs of said output circuit, wherein said logic circuit partitions said output circuit into at least a first portion and a second portion to perform said logical 'NAND' function.

5. The logic circuit of claim 1, wherein the one or more valid states comprises one of a precharge state, a true state and a false state.

6. A method for performing a near simultaneous comparison of multiple bits using a logical XOR function in a manner that avoids an XOR function hazard of the logical XOR function, said method comprising the steps of:

generating a plurality of dual-rail domino signal pairs from a plurality of input signals in a manner that avoids an unstable state in a logical XOR circuit to avoid the XOR function hazard in the logical XOR circuit; and

performing the logical XOR function on the plurality of said dual-rail domino signal pairs in the logical XOR circuit to perform the near simultaneous comparison of bits without the logical XOR circuit entering the unstable state.

7. The method of claim 6, wherein each of the plurality of dual-rail domino signal pairs comprises a first complementary dual-rail domino value and a second complementary dual-rail domino value.

8. The method of claim 7, wherein each of said first and said second complementary dual-rail domino values allow said logical XOR circuit to transition from a first stable state to a second stable state without having to transition through said unstable state when performing the near simultaneous comparison of multiple bits.

9. A circuit to perform a substantially simultaneous comparison of multiple bits, comprising:

an encoder circuit to receive a plurality of input signals and generate a plurality of dual-rail domino output signals from the plurality of input signals in a manner that prevents of each of said plurality of dual-rail domino output signals from entering an invalid state; and

an exclusive OR (XOR) logic circuit not subject to an XOR function hazard to perform the substantially simultaneous comparison of multiple bits in the plurality of dual-rail domino output signals from said encoder circuit.

10. The circuit of claim 9, wherein said encoder circuit comprises,

a plurality of first encoder circuits to generate a plurality of first dual-rail domino output signals from a plurality of first input signals; and

a plurality of second encoder circuits to generate a plurality of second dual-rail domino output signals from a plurality of second input signals.

11. The circuit of claim 10, wherein each of the plurality of first encoder circuits comprises,

a first circuit cross-coupled to a second circuit, wherein said second circuit receives at least one value of said first input signal and said first circuit receives a clock signal, wherein said first circuit and said second circuit convert the at least one value of said first input signal to one of said first dual-rail domino output values in a manner that prevents generation of an invalid output state for each of the first dual-rail domino output signals to prevent a logic function hazard in said XOR circuit.

12. The circuit of claim 10, wherein each of the plurality of second encoder circuits comprises,

a first circuit cross-coupled to a second circuit wherein said second circuit receives at least one value of said second input signal and said first circuit receives said clock signal, wherein said first circuit and said second circuit convert the at least one value of said second input signal to one of said second dual-rail domino output signals in a manner that prevents generation of an invalid output state to prevent a logic function hazard in said XOR circuit.

13. The circuit of claim 9, wherein said encoder circuit generates the plurality of dual-rail domino signals for each of said plurality of input signals when said clock signal enters its "B" phase.

14. The circuit of claim 9, wherein said XOR logic circuit comprises,

a plurality of dual-rail dynamic logic circuits each with or without a series-evaluate transistor and each of the plurality of dual-rail dynamic logic circuits having a first pull-down stack and a second pull-down stack coupled in parallel between a ground node and a dynamic node, wherein the plurality of first pull-down stacks and the plurality of second pull-down stacks in the plurality of dual-rail dynamic logic circuits perform said XOR function on said plurality of dual-rail domino output signals of said static to dynamic converter circuit.

15. The circuit of claim 14, wherein said XOR logic circuit further comprises,

a first plurality of input nodes and a second plurality input nodes to receive a plurality of outputs of said first encoder circuit; and

a third plurality of input nodes and a fourth plurality of input nodes to receive a plurality of outputs of said second encoder circuit, wherein each of said plurality of second input nodes and each of said plurality of third input nodes are each coupled to one of said plurality of first pull-down stacks and each of said plurality of first input nodes and each of said plurality of fourth input nodes are coupled to one of said plurality of second pull-down stacks.

16. The circuit of claim 9, further comprising a clocked storage element coupled to an output of said XOR circuit to store a result of said XOR function for at least one clock cycle.

17. The circuit of claim 16, wherein said clocked storage element comprises a level sensitive latch.

18. An XOR logic circuit to compare multiple bits comprising,

an encoder circuit to encode a plurality of input values asserted on a plurality of input nodes of said encoder circuit into a plurality of output value pairs; and

an output circuit to perform a logical XOR function on the plurality of output value pairs to perform the comparison of the multiple bits, wherein each of the plurality of output value pairs each have three states to allow said XOR logic circuit to operate without an XOR function hazard when comparing the multiple bits.

19. The XOR logic circuit of claim 18, wherein said three valid states of each of said plurality of output value pairs comprises a precharge state, a false state and a true state.

20. The XOR logic circuit of claim 19, wherein said encoder circuit utilizes an implied inversion technique to encode each of said plurality of input values.

21. The XOR logic circuit of claim 19, wherein each of said plurality of output value pairs comprise complementary data values when said encoder circuit is in an evaluate state.

22. The XOR logic circuit of claim 18, wherein each of said plurality of output values comprise like data values when said encoder circuit is in a precharge state.

23. The XOR logic circuit of claim 18, wherein said output circuit comprises, a plurality of dual-rail dynamic logic circuits each with or without a series-evaluate transistor and each having a first pull-down stack and a second pull-down stack coupled in parallel between a ground node and a dynamic node, wherein said first pull-down stack and said second pull-down stack perform said logical XOR function on one of said plurality of output value pairs.